REMARKS

The foregoing amendments are made to correct minor translational errors and to meet United States requirements as to form. No new matter is added.

Respectfully submitted,

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PATENT
Attorney Docket No. 401352

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

SHINTANI et al.

Application No.	Unassigned	Art Unit:	Unassigned
Filed:	August 22, 2001	Examiner:	Unassigned

For: METHOD OF FABRICATING SEMICONDUCTOR DEVICE AND WAFER TREATMENT APPARATUS EMPLOYED THEREFOR AS WELL AS SEMICONDUCTOR DEVICE

AMENDMENTS TO SPECIFICATION, CLAIMS, AND ABSTRACT MADE VIA PRELIMINARY AMENDMENT

Amendments to the paragraph beginning at page 1, line 15:

High performance is required particularly ~~to~~ in a transistor employed for a logic circuit or a system LSI (large-scale integrated circuit) among semiconductor devices. In order to satisfy this requirement, the thickness of a gate ~~insulator~~ insulation film of the transistor is set to not more than 3 nm. Further, a development ~~is~~ has recently been made for reducing the thickness of the gate ~~insulator~~ insulating film below 2 nm.

Amendments to the paragraph beginning at page 2, line 10:

The polysilicon film is etched through the mask member in an atmosphere prepared by converting a gas mixture containing Cl_2 and O_2 or HBr, Cl_2 and O_2, for example, ~~to~~ into a plasma ~~thereby~~, patterning the gate electrode. In this patterning, a reaction product adheres to the side wall surfaces of the gate electrode and the surface of

the mask member. After formation of the gate electrode, the reaction product adhering to the gate electrode is removed by wet cleaning.

Amendments to the paragraph beginning at page 2, line 17:

It is known that the reaction product is mainly composed of a silicon oxide such as SiO_xCl_y or SiO_xBr_y when the polysilicon film is etched by converting the gas mixture containing Cl_2 and O_2 or HBr, Cl_2, and O_2 to a plasma ~~in particular~~.

Amendments to the paragraph beginning at page 3, line 26:

In this case, the etched portion may not be fully filled ~~up~~ but ~~define~~ produce a void when the gate electrode 103 is covered with an interlayer isolation film, ~~to~~ and reduce the reliability of the semiconductor device.

Amendments to the existing claims:

1. (Amended) A method of fabricating a semiconductor device comprising a wafer treatment ~~step performing prescribed treatment on~~ of a first part of the wafer having a ~~prescribed~~ first etching property and a second part of the wafer having ~~an~~ a second etching property different from ~~said prescribed~~ the first etching property, ~~formed on a semiconductor substrate,~~ in a chamber with a gas for etching, ~~wherein~~ including:

~~said wafer treatment step includes an etching gas supply step of~~ introducing ~~said~~ the gas for etching into ~~said~~ the chamber, and

assuming that a time between introduction of ~~said~~ the gas for etching into ~~said~~ the chamber and starting of etching of ~~said~~ the first part of the wafer is ~~referred to as~~ a first starting time, and a time between introduction of ~~said~~ the gas for etching into ~~said~~ the chamber and starting of etching of ~~said~~ the second part of the wafer is ~~referred to as~~ a second starting time, longer than said first starting time, ~~a time for carrying out said~~ supplying the gas for etching ~~gas supply step is~~ for a time longer than ~~said~~ the first starting time ~~and~~ but shorter than ~~said~~ the second starting time.

2. (Amended) The method of fabricating a semiconductor device according to claim 1, wherein the time difference between ~~said~~ the first starting time and ~~said~~ the second starting time is not more than about 5 seconds.

3. (Amended) The method of fabricating a semiconductor device according to claim 1, further comprising ~~steps of~~:

forming ~~an insulator~~ a gate insulating film on ~~said~~ the semiconductor substrate, and

forming a ~~conductive region~~ gate electrode on ~~said insulator~~ the insulating film, wherein

~~said step of forming said insulator film includes a step of forming a gate insulator film,~~

~~said step of forming said conductive region includes a step of forming a gate electrode part on said gate insulator film,~~

~~said~~ the first part of the wafer contains a reaction product generated before forming ~~said~~ the gate electrode ~~part for~~, covering the ~~surface of said~~ gate ~~insulator~~ insulating film and the ~~surface of said~~ gate electrode ~~part~~,

~~said~~ the second part includes said gate ~~insulator~~ insulating film, and

~~said~~ the gas for etching includes hydrofluoric acid ~~gas~~.

4. (Amended) The method of fabricating a semiconductor device according to claim 1, ~~wherein said wafer treatment step includes an added gas supply step of~~ including introducing a reaction accelerating gas into the chamber before introducing the gas for etching for ~~further~~ reducing ~~said~~ the first starting time ~~into said chamber before said etching gas supply step~~.

5. (Amended) The method of fabricating a semiconductor device according to claim 4, ~~wherein said added gas supply step and said etching gas supply step are~~ including alternately ~~carried out in said wafer treatment step~~ introducing the reaction accelerating gas and the gas for etching.

6. (Amended) The method of fabricating a semiconductor device according to claim 4, ~~wherein said added gas supply step is continuously carried out also after said etching gas~~ including continuously adding the reaction accelerating gas after starting supply ~~step is started in said wafer treatment step~~ of the gas for etching.

7. (Amended) The method of fabricating a semiconductor device according to claim 1, ~~wherein said wafer treatment step includes an evacuation step of~~ including evacuating ~~said~~ the chamber, ~~and said evacuation step is~~ but not ~~carried out at least~~ while the gas for etching ~~gas supply step~~ is ~~carried out~~ being supplied.

8. (Amended) The method of fabricating a semiconductor device according to claim 1, further comprising ~~steps of~~:

forming a conductive layer on ~~said semiconductor substrate through~~ a gate ~~insulator~~ insulating film on the semiconductor substrate,

forming a layer for defining a mask on ~~said~~ the conductive layer,

etching ~~said~~ the conductive layer through a mask of ~~said~~ the layer for defining a mask, thereby forming a gate electrode, and

removing ~~said~~ the layer for defining a mask remaining on ~~said~~ the gate electrode after formation of ~~said~~ the gate electrode, wherein

~~said wafer treatment step includes a step of removing said layer for defining a mask,~~

~~said~~ the first part of the wafer includes ~~said~~ the layer for defining a mask,

~~said~~ the second part of the wafer includes ~~said~~ the gate insulator film, and

hydrofluoric acid gas is supplied as the gas for etching ~~gas in said etching gas supply step~~ to remove the layer for defining a mask.

9. (Amended) The method of fabricating a semiconductor device according to claim 8, ~~wherein said etching gas supply step is repetitively carried out in said wafer treatment step~~ including repeatedly supplying the gas for etching.

10. (Amended) The method of fabricating a semiconductor device according to claim 9, ~~wherein said wafer treatment step includes an evacuation step~~ including evacuating ~~said~~ the chamber, and ~~said~~ alternatively supplying the gas for etching ~~gas supply step~~ and ~~said evacuation step are alternately carried out~~ evacuating the chamber.

11. (Amended) A wafer treatment apparatus for ~~performing prescribed treatment on~~ treating a first part of the wafer having a ~~prescribed~~ first etching property and a second part of the wafer having ~~an~~ a second etching property, different from ~~said prescribed~~ the first etching property, ~~formed on a wafer,~~ with a gas for etching, comprising:

a chamber ~~storing said~~ for holding a wafer;

an etching gas supply part supplying ~~said~~ the gas for etching into said chamber; and

a control part controlling supply of ~~said~~ the gas for etching from said etching gas supply part into said chamber, wherein said control part ~~has~~, assuming that a time between introduction of ~~said~~ the gas for etching into said chamber and starting of etching of ~~said~~ the first part of the wafer is ~~referred to as~~ a first starting time and a time between introduction of ~~said~~ the gas for etching into said chamber and starting of etching of ~~said~~ the second part of the wafer is ~~referred to as~~ a second starting time, longer than ~~said~~ the first starting time, ~~a function of supplying said~~ supplies the gas for etching from said etching gas supply part into said chamber ~~by~~ for a time longer than ~~said~~ the first starting time ~~and~~ but shorter than ~~said~~ the second starting time.

12. (Amended) The wafer treatment apparatus according to claim 11, wherein the time difference between ~~said~~ the first starting time and ~~said~~ the second starting time is not more than about 5 seconds.

13. (Amended) The wafer treatment apparatus according to claim 11, further comprising ~~:~~ an added gas supply part supplying a reaction accelerating gas, for reducing ~~said~~ the first starting time, into said chamber, wherein said control part ~~includes a function of supplying said~~ supplies the reaction accelerating gas from said added gas supply part into said chamber before supplying ~~said~~ the gas for etching.

14. (Amended) The wafer treatment apparatus according to claim 13, wherein said control part ~~includes a function of~~ alternately ~~supplying said~~ supplies the gas for etching and ~~said~~ the reaction accelerating gas.

15. (Amended) The wafer treatment apparatus according to claim 13, wherein said control part ~~includes a function of supplying said~~ supplies the reaction accelerating gas ~~also~~ while supplying ~~said~~ the gas for etching.

16. (Amended) The wafer treatment apparatus according to claim 11, further comprising an evacuation part evacuating said chamber, wherein said control part ~~includes a function of not operating~~ prevents said evacuation part ~~at least~~ from operating while supplying ~~said~~ the etching gas.

17. (Amended) A ~~cleaning~~ method of cleaning a wafer after formation of a gate electrode, including removing a reaction product formed by etching with hydrofluoric acid gas, after forming ~~a~~ the gate electrode that has been patterned by ~~said~~ the etching with a mask on a semiconductor substrate, through a gate insulating film.

18. (Amended) The cleaning method ~~after formation of a gate electrode~~ according to claim 17, ~~wherein the time for~~ including removing ~~said~~ the reaction product with ~~said~~ hydrofluoric acid gas ~~is~~ within ~~the~~ a reaction time difference between a time when ~~said~~ the reaction product is ~~scraped~~ etched by ~~said~~ the hydrofluoric acid gas and a time when ~~said~~ the gate ~~insulator~~ insulating film is ~~scraped~~ etched by the hydrofluoric acid gas.

19. (Amended) The cleaning method ~~after formation of a gate electrode~~ according to claim 18, wherein ~~said~~ the reaction time difference is repetitively set, thereby removing ~~said~~ the reaction product with ~~said~~ the hydrofluoric acid gas.

20. (Amended) The cleaning method ~~after formation of a gate electrode~~ according to claim 19, wherein ~~said~~ a semiconductor substrate ~~formed with said~~ including the gate electrode is set in a chamber, and ~~said~~ the reaction time difference is repetitively

set by ~~repeating steps of~~ repeatedly evacuating ~~said~~ the chamber and charging ~~said~~ the chamber with ~~said~~ the hydrofluoric acid gas.

Amendments to the abstract:

ABSTRACT OF THE DISCLOSURE

In a wafer treatment apparatus, a hydrofluoric acid gas supply pipe and an evacuation pipe are connected to a chamber ~~storing~~ holding a wafer for performing ~~prescribed~~ a treatment. A control part ~~is provided for controlling~~ controls supply of hydrofluoric acid gas. The control part sets a time for supplying the hydrofluoric acid gas into the chamber ~~to be~~ that is longer than a time ~~up to~~ until starting of etching of a reaction product and shorter than a time ~~up to~~ until starting of etching of a gate ~~insulator~~ insulating film. Thus, ~~only~~ the reaction product can be substantially etched without etching the gate ~~insulator~~ insulating film.